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From:	Kevin J. Zilka		

Docket No.: NAI1P069/99.074.01 **App. No: 09/609,690**

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Practitioner's Docket No. NAI1P069/99.074.01 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Wu et al.

Application No.: 09/609,690 Group No.: 2157
Filed: 7/5/2000 Examiner: Gold, Avi M.
For: HIGH PERFORMANCE PACKET PROCESSING USING A GENERAL PURPOSE PROCESSOR

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Commissioner for Patents
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Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

1. Transmitted herewith is a SUPPLEMENTAL APPEAL BRIEF in this application, with respect to the Notice of Appeal filed on September 27, 2004, and the original Appeal Brief filed September 29, 2004.

2. STATUS OF APPLICANT

This application is on behalf of other than a small entity.

CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*
*(When using Express Mail, the Express Mail label number is **mandatory**;*
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Date: 7/7/2005

Erica L. Farlow
Signature

Erica L. Farlow
(type or print name of person certifying)

** Only the date of filing (' 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under ' 1.8 continues to be taken into account in determining timeliness. See ' 1.703(f). Consider "Express Mail Post Office to Addressee" (' 1.10) or facsimile transmission (' 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.*

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 C.F.R. § 1.17(c), the fee for filing the Appeal Brief has already been paid. However, the commissioner is authorized to charge any fees that may be due to deposit account 50-1351 (NAI1P069).

4. EXTENSION OF TERM

The proceedings herein are for a patent application and the provisions of 37 C.F.R. § 1.136 apply.

Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal brief fee	$0.00
Extension fee (if any)	$0.00

6. PAYMENT OF FEES

Applicant believes no fees are due in connection with the filing of this paper because the fees were paid with the previous submission. However, the commissioner is authorized to charge any fees that may be due to deposit account 50-1351 (NAI1P069).

7. FEE DEFICIENCY

If any additional extension and/or fee is required, and if any additional fee for claims is required, charge Deposit Account No. 50-1351 (Order No. NAI1P069).

Signature of Practitioner

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San Jose, CA 95172-1120
USA

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Wu et al.

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TRANSMISSION

✓ facsimile transmitted to the Patent and Trademark Office, (703) 872-9306.

Signature

Date: 7/7/2005

Erica L. Farlow
(type or print name of person certifying)

** Only the date of filing (' 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under ' 1.8 continues to be taken into account in determining timeliness. See ' 1.703(f). Consider "Express Mail Post Office to Addressee" (' 1.10) or facsimile transmission (' 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.*

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4. EXTENSION OF TERM

The proceedings herein are for a patent application and the provisions of 37 C.F.R. § 1.136 apply.

Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal brief fee	$0.00
Extension fee (if any)	$0.00

6. PAYMENT OF FEES

Applicant believes no fees are due in connection with the filing of this paper because the fees were paid with the previous submission. However, the commissioner is authorized to charge any fees that may be due to deposit account 50-1351 (NAI1P069).

7. FEE DEFICIENCY

If any additional extension and/or fee is required, and if any additional fee for claims is required, charge Deposit Account No. 50-1351 (Order No. NAI1P069).

Signature of Practitioner

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USA

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of	)
	)
Wu et al.	) Group Art Unit: 2157
	)
Application No. 09/609,690	) Examiner: Gold, Avi M.
	)
Filed: 07/05/00	) Docket No. NAI1P069_99.074.01
	)
For: HIGH PERFORMANCE PACKET PROCESSING USING A GENERAL PURPOSE PROCESSOR	) Date: July 7, 2005)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

SUPPLEMENTAL APPEAL BRIEF (37 C.F.R. § 41.37)

This brief is in furtherance of the Notice of Appeal, filed in this case on September 27, 2004, and the original Appeal Brief filed September 29, 2004. This brief is further in response to the Office Action mailed April 20, 2004 for the purpose of re-instatement of the related appeal.

The fees required under § 1.17, and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. § 41.37(c)(i)):

I REAL PARTY IN INTEREST
II RELATED APPEALS AND INTERFERENCES
III STATUS OF CLAIMS

IV STATUS OF AMENDMENTS

V SUMMARY OF CLAIMED SUBJECT MATTER

VI ISSUES

VII ARGUMENTS

VIII APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

IX APPENDIX LISTING ANY EVIDENCE RELIED ON BY THE APPELLANT IN THE APPEAL

The final page of this brief bears the practitioner's signature.

I REAL PARTY IN INTEREST (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is McAfee, Inc.

II RELATED APPEALS AND INTERFERENCES (37 C.F.R. § 41.37(c) (1)(ii))

With respect to other prior or pending appeals, interferences, or related judicial proceedings that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, there is no such prior or pending appeals, interferences, or related judicial proceedings.

III STATUS OF CLAIMS (37 C.F.R. § 41.37(c) (1)(iii))

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-18, and 30

B. STATUS OF ALL THE CLAIMS IN APPLICATION

1. Claims withdrawn from consideration: None
2. Claims pending: 1-18, and 30
3. Claims allowed: None
4. Claims rejected: 1-18, and 30

C. CLAIMS ON APPEAL

The claims on appeal are: 1-18, and 30

See additional status information in the Appendix of Claims.

IV STATUS OF AMENDMENTS (37 C.F.R. § 41.37(c)(1)(iv))

As to the status of any amendment filed subsequent to final rejection, there are no such amendments after final.

V SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. § 41.37(c)(1)(v))

With respect to a summary of Claim 1 et al., as shown in Figure 1, a packet processing device is provided including a control logic processor (e.g. item 10 of Figure 1) for filtering packets according to a set of stored rules and an arithmetic logic processor (e.g. item 20 of Figure 1) for executing packet processing instructions based on the content of the packet. In use, the control logic processor spawns a new thread for each incoming packet, relieving the arithmetic logic processor of the need to do so. The control logic processor and the arithmetic logic processor are integrated via a thread queue. The control logic processor assigns a policy to each incoming packet. See operation 202 of Figure 2, for example. A policy action table stores one or more policy instructions which may be easily changed to update policies to be implemented. The policy action table maps a virtual packet flow identification code to the physical memory address of an action code and a state block associated to the identification code. The arithmetic logic processor processes a packet based on the stored policy assigned to that packet. Note page 4, line 20 – page 9, line 25, for example.

With respect to a summary of Claim 30 et al., the above summary is incorporated, at least in part, by reference. Further provided is an apparatus that includes a control logic unit coupled to an input and the policy condition table for feeding an arithmetic logic unit, which is in turn coupled to the policy action table and the state block for generating an output. Note, for example, items 10 and 20 of Figure 1, and the accompanying description found on page 3, line 10 – page 4, line 20.

VI ISSUES (37 C.F.R. § 41.37(c)(1)(vi))

Following, under each issue listed, is a concise statement setting forth the corresponding ground of rejection.

Issue # 1: The Examiner has rejected Claims 1-16 and 30 under 35 U.S.C. 102(e) as being anticipated by Kadambi et al., U.S. Patent No. 6,850,521.

Issue # 2: The Examiner has rejected Claims 17 and 18 under 35 U.S.C. 103(a) as being unpatentable over Kadambi in view of Scales, U.S. Patent No. 5,761,729.

VII ARGUMENTS (37 C.F.R. § 41.37(c)(1)(vii))

The claims of the groups noted below do not stand or fall together. In the present section, appellant explains why the claims of each group are believed to be separately patentable.

Issue #1:

The Examiner has rejected Claims 1-16 and 30 under 35 U.S.C. 102(e) as being anticipated by Kadambi et al., U.S. Patent No. 6,850,521.

Group #1: Claims 1, 2, and 16

Specifically, with respect to Claim 1, the Examiner relies on the following excerpt from Kadambi to meet appellant's claimed "second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit."

> "In other words, **a logical AND operation is performed with the filter mask, having the selected fields enabled, and the packet. If there is a match, the matching entries are applied to rules tables 22**, in order to determine which specific actions will be taken. Since there are a limited number of fields in the rules table, and since particular rules must be applied for various types of packets, the rules table requirements are minimized by setting all incoming packets to be "tagged" packets; all untagged packets, therefore, are subject to 802.1Q tag insertion, in order to reduce the number of entries which are necessary in the rules table. This action eliminates the need for entries regarding handling of untagged packets. It should be noted that specific packet types are defined by various IEEE and other networking standards, and will not be defined herein." (Col. 35, lines 24-38- emphasis added)

Appellant respectfully asserts that the above excerpt from Kadambi merely teaches applying a rules table to entries when a packet and filter mask match (see emphasized excerpt above). There is clearly no disclosure of "a second data processing unit" (emphasis added), as claimed by

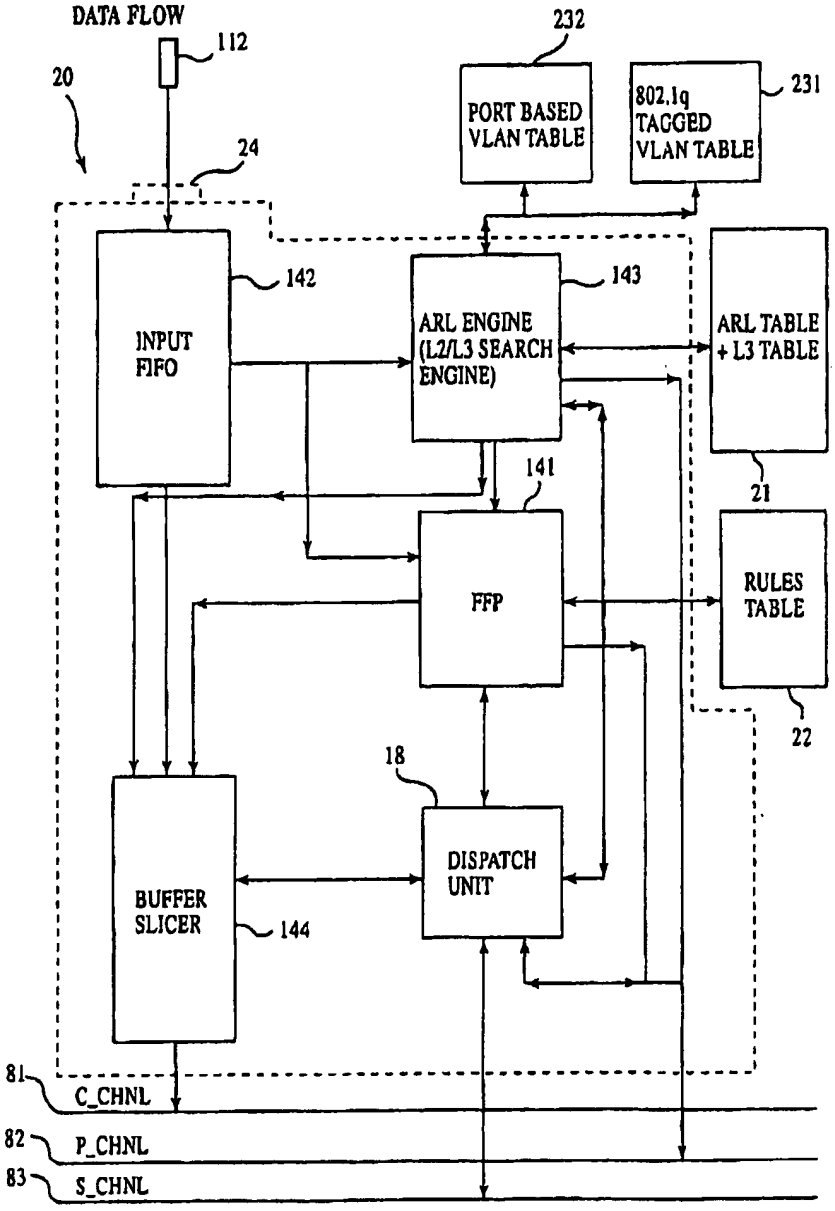
appellant. In fact, Kadambi teaches an SOC (switch-on-chip) that operates in a free running manner without communicating with the CPU (see Col. 5, lines 15-18).

Further, Kadambi also fails to teach a second data processing unit that "process[es] incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit." Simply nowhere in Kadambi is there any disclosure of applying instructions based on a thread of the packet, let alone in the above excerpt which teaches that the packet is only applied to the rules table if the packet matches a filter mask (see emphasize excerpt above).

In addition, the Examiner has relied on Figures 14 and 15 from Kadambi to make a prior art showing of appellant's claimed "data bus connecting the addressable memory unit and the first and second data processing units." Appellant respectfully asserts the disclosure associated with Figure 15 expressly states that "the filter masks, rules tables, and logic, while programmable by the CPU 52, do not rely upon CPU 52 for processing and calculation thereof" (see Col. 35, lines 51-56). Again, appellant emphasizes that Kadambi teaches an SOC (switch-on-chip) that operates in a free running manner without communicating with the CPU (see Col. 5, lines 15-18). Thus, Kadambi does not teach "the first and second data processing units," in the context claimed by appellant.

Still yet, it seems the Examiner has relied on Kadambi's "input FIFO" (see Figures 14 and 15) to meet appellant's claimed addressable memory unit connected to first and second processing units by way of a data bus. Appellant asserts that the input FIFO's in both figures relied on by the Examiner are not attached to first and second data processing units, but rather are simply a part of an EPIC module (see Figure 14, element 20 below), wherein the EPIC module itself is connected to channels (see Figure 14, elements 81-83 below). Thus, there is clearly no data bus disclosed in Kadambi, and especially not in the manner claimed by appellant.

Fig.14



The Examiner is reminded that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference.

Verdegaal Bros. v. Union Oil Co. Of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, the identical invention must be shown in as complete detail as contained in the claim. Richardson v. Suzuki Motor Co.868 F.2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim.

This criterion has simply not been met by the Kadambi reference, especially in view of the arguments made hereinabove.

Group #2: Claims 3 and 5

With respect to the present group, the Examiner relies on the following excerpt from Kadambi to make a prior art showing of appellant's claimed "policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy."

> "Referring once again to FIG. 14, after. FFP 141 applies appropriate configured filters and results are obtained from the appropriate rules table 22, logic 1411 in FFP 141 determines and takes the appropriate action. The filtering logic can discard the packet, send the packet to the CPU 52, modify the packet header or IP header, and recalculate any IP checksum fields or takes other appropriate action with respect to the headers. The modification occurs at buffer slicer 144, and the packet is placed on C channel 81." (Col. 35, lines 57-64)

After careful review of such excerpt, it is clear that Kadambi fails to disclose, teach or suggest appellant's specific claim language. For instance, the Examiner relies on Kadambi's "filtering logic" to meet appellant's claimed "policy action table." Simple filtering logic in no way meets the claimed table, and especially not a table that "stores at least one data processing policy." Only appellant teaches and claims a policy action table connected to a data bus and a addressable memory unit that stores at least one data processing policy.

Again, appellant respectfully asserts that Kadambi does not meet all of appellant's claim language, for the reasons set forth hereinabove.

Group #3: Claim 4

With respect to Claim 4, the Examiner relies on col. 31, lines 20-34 from Kadambi to make a prior art showing of appellant's claimed "second address pointer element for identifying the location in said addressable memory unit of a state block." Specifically, the Examiner relies on Kadambi's FFP and states that such is essentially a state machine. Appellant respectfully disagrees with this assertion as there is simply no suggestion in Kadambi of any sort of address pointer that identifies the location of a state block in addressable memory. Instead, the above excerpt from Kadambi merely teaches applying different filters in a state machine.

Again, appellant respectfully asserts that Kadambi does not meet all of appellant's claim language, for the reasons set forth hereinabove.

Group 4: Claims 6-14

With respect to Claim 6, the Examiner relies on col. 35, lines 24-65 from Kadambi to make a prior art showing of appellant claimed technique "wherein said first data processing unit comprises logic for matching a first incoming packet to a stored first rule and for generating a first thread if the first incoming packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table." Appellant respectfully asserts that Kadambi only teaches applying packets to a rules table if the packet matches a filter mask (see Col. 35, lines 24-28), and tagging all packets (see Col. 35, lines 31-32). Thus, there is clearly no teaching of generating a thread if the first incoming packet matches a first rule, as claimed by appellant.

Again, appellant respectfully asserts that Kadambi does not meet all of appellant's claim language, for the reasons set forth hereinabove.

Group 4: Claim 15

With respect to Claim 15, the Examiner has relied on col. 31, lines 34-45 and col. 35, lines 24-65 of Kadambi to make a prior art showing of appellant's claimed "memory unit connected to said first data processing unit and to said second data processing unit, said memory unit adapted to temporarily store packets before processing by said second data processing unit." Specifically, the Examiner has stated that Kadambi discloses packets stored within FFP. Appellant asserts that the above excerpt expressly teaches that "FFP 141 is shown to include filter database containing filter masks therein" (Col. 35, lines 46-47). Thus, since in Kadambi, the FFP is only taught to include filter masks and not that it temporarily stores packets, such an excerpt does not meet appellant's specific claim language, namely "said memory unit adapted to temporarily store packets."

Again, appellant respectfully asserts that Kadambi does not meet all of appellant's claim language, for the reasons set forth hereinabove.

Group 5: Claim 30

With respect to Claim 30, appellant notes numerous deficiencies (including those set forth hereinabove regarding related claims). For example, the Examiner relies on col. 31, lines 24-45 and col. 35, lines 24-64 to make a prior art showing of appellant's claimed technique "wherein the apparatus includes a control logic unit couples to an input and the policy condition table for feeding an arithmetic logic unit, which is in turn coupled to the policy action table and the state block for generating an output." Appellant respectfully asserts that the Kadambi reference does not teach an arithmetic logic unit, in the manner claimed by appellant, but instead merely teaches applying filters to packets (col. 31, lines 24-45) and applying packets to rules tables when the packet matches a filter mask (Col. 35, lines 24-64). Further, Kadambi also does not teach

utilizing a state block for generating output, but instead simply discloses using a rules table to determine which actions will be taken with respect to the packet (see Col. 35, lines 26-28).

Issue #2:

The Examiner has rejected Claims 17 and 18 under 35 U.S.C. 103(a) as being unpatentable over Kadambi in view of Scales, U.S. Patent No. 5,761,729.

Group #1: Claims 17 and 18

These claims are deemed allowable for the reasons set forth hereinabove with respect to Claim 1.

In view of the remarks set forth hereinabove, all of the independent claims are deemed allowable, along with any claims depending therefrom.

VIII APPENDIX OF CLAIMS (37 C.F.R. § 41.37(c)(1)(viii))

The text of the claims involved in the appeal (along with associated status information) is set forth below:

1. (Previously Presented) An apparatus for processing data packets, comprising:

a first data processing unit adapted to filter incoming packets;

an addressable memory unit in which a plurality of instruction sets for packet processing are stored;

a second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit; and

a data bus connecting the addressable memory unit and the first and second data processing units.

2. (Original) The apparatus of claim 1, further comprising a policy condition table connected to said first data processing unit, said policy condition table having a plurality of rules stored therein.

3. (Original) The apparatus of claim 1, further comprising a policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy.

4. (Original) The apparatus of claim 3, wherein at least one of said policies comprises:

a first address pointer element for identifying the location in said addressable memory unit of one of said plurality of instruction sets, and

a second address pointer element for identifying the location in said addressable memory unit of a state block.

5. (Original) The apparatus of claim 3, wherein said first data processing unit assigns a thread to each said incoming packet, wherein said thread corresponds to one of said policies stored in said policy action table.

6. (Original) The apparatus of claim 3, wherein said first data processing unit comprises logic for matching a first incoming packet to a stored first rule and for generating a first thread if the first incoming packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table.

7. (Original) The apparatus of claim 6, wherein said second data processing unit is adapted to process the first incoming packet according to said data processing policy corresponding to said first thread.

8. (Original) The apparatus of claim 6, wherein said data processing policy comprises a first address pointer to a starting address of a first set of instructions and a second address pointer to a starting address of a state block stored in said addressable memory unit, said state block used by said first set of instructions for processing the first incoming packet.

9. (Original) The apparatus of claim 6, wherein said thread is assigned to said first incoming packet based on said first rule.

10. (Original) The apparatus of claim 6, wherein said first processing unit further comprises logic for matching a second incoming packet to a stored second rule and for generating a second thread if the second incoming packet matches the second rule, said second thread identifying the location of one of said at least one data processing policy in said policy action table.

11. (Original) The apparatus of claim 10, wherein said second data processing unit is adapted to process the second incoming packet according to said data processing policy corresponding to said second thread.

12. (Original) The apparatus of claim 10, wherein said second thread is assigned to said second incoming packet based on said second rule.

13. (Previously Presented) The apparatus of claim 3, wherein said first processing unit further comprises logic for matching a plurality of incoming packets to a stored corresponding plurality of rules and for generating a thread for each packet that matches one of said plurality of rules, each said thread identifying the location of one of said at least one data processing policy in said policy action table.

14. (Original) The apparatus of claim 13, wherein the second data processing unit is adapted to process each packet according to said data processing policy corresponding to said thread associated with said packet.

15. (Original) The apparatus of claim 13, further comprising a memory unit connected to said first data processing unit and to said second data processing unit, said memory unit adapted to temporarily store packets before processing by said second data processing unit.

16. (Original) The apparatus of claim 1, wherein said second data processing unit comprises a plurality of general purpose processors for executing instructions in parallel.

17. (Original) The apparatus of claim 16, wherein at least one said general purpose processor comprises a complex instruction set computer processor.

18. (Original) The apparatus of claim 16, wherein at least one said general purpose processor comprises a reduced instruction set computer processor.

19. - 29. (Cancelled)

30. (Previously Presented) An apparatus for processing data packets, comprising:

a first data processing unit adapted to filter incoming packets;

an addressable memory unit in which a plurality of instruction sets for packet processing are stored;

a second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit; and

a data bus connecting the addressable memory unit and the first and second data processing units;

wherein a policy condition table is connected to said first data processing unit, said policy condition table having a plurality of rules stored therein;

wherein a policy action table is connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy;

wherein said first data processing unit comprises logic for matching a first incoming packet to a stored first rule and for generating a first thread if the first incoming packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table;

wherein said second data processing unit is adapted to process the first incoming packet according to said data processing policy corresponding to said first thread;

wherein said data processing policy comprises a first address pointer to a starting address of a first set of instructions and a second address pointer to a starting address of a state block stored in said addressable memory unit,

said state block used by said first set of instructions for processing the first incoming packet;

wherein said first processing unit further comprises logic for matching a second incoming packet to a stored second rule and for generating a second thread if the second incoming packet matches the second rule, said second thread identifying the location of one of said at least one data processing policy in said policy action table;

wherein said second data processing unit is adapted to process the second incoming packet according to said data processing policy corresponding to said second thread;

wherein a memory unit is connected to said first data processing unit and to said second data processing unit, said memory unit adapted to temporarily store packets before processing by said second data processing unit;

wherein said second data processing unit comprises a plurality of general purpose processors for executing instructions in parallel;

wherein the apparatus includes a control logic unit coupled to an input and the policy condition table for feeding an arithmetic logic unit, which is in turn coupled to the policy action table and the state block for generating an output.

IX APPENDIX LISTING ANY EVIDENCE RELIED ON BY THE APPELLANT IN THE APPEAL (37 C.F.R. § 41.37(c)(1)(ix))

There is no such evidence.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 971-2573. For payment of any additional fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NAI1P069).

Respectfully submitted,

By: _____ Date: 7/7/05

Kevin J. Zilka

Reg. No. 41,429

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